DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 3/24/08 have been fully considered but they are not persuasive.

2. Applicant argues that in previous Office communications claims 36-38 and 39 were rejected under U.S.C. 103 in view of a primary reference (Kondo) and a secondary reference (Davis, Gardner and/or Nelson) and that claims 41 and 42 were found allowable in substance. Therefore, Applicant concludes, the current rejection appears untenable.

3. In response, it should be pointed out the fact that during the original prosecution of the patent the Examiner overlooked a teaching in a prior art document, does not prevent the Examiner from applying that teaching during further prosecution of the application.

4. Referring to Kondo's fig. 1B, Applicant further argues that the chip area consumed to implement the field plate in the structure includes the area of the field plate 7, plus the area of the first resistor contact 4-1, plus the area of the second resistor contact 4-2. By contrast, Applicant concludes, in applicant's claimed field plate implementation, the chip area consumed is the area of the field plate, plus the area of the second resistor contact 82 and that the first resistor contact 46 does not add to the chip area consumed since it resides below the field plate itself.

5. In response, as stated in the previous Office Action the embodiment which was relied upon is shown in Kondo's figs. 4-10 rather than the embodiment shown in fig. 1B (see page 10, lines 2-10 of Applicant's Remarks). Furthermore, it is noted that the features upon which applicant relies (i.e., the chip area consumed is the area of the field plate, plus the area of the

second resistor contact 82 and that the first resistor contact 46 does not add to the chip area consumed …) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to this Office Action, Applicant is urged to specifically point out the limitation or limitations which are not taught or disclosed by Kondo (see the embodiment shown in figs. 4-10).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 36-39, 41 and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Kondo USPN 4,609,935

Kondo discloses a method for the manufacture of an integrated circuit including a field plated resistor comprising:

a) forming a resistor body 35 (fig. 6) in a semiconductor substrate, the resistor body having first and second contact regions 40-1/40-2 (fig. 7);

b) a first insulating layer (col. 6, lines 46-49) over the resistor body (fig. 7), the first insulating layer approximately coextensive with the resistor body and having a top surface and a bottom surface;

c) forming a contact window in the first insulating layer (col. 6, lines 46-49) and extending from the top surface of the first insulating layer through the first insulating layer through the first insulating layer to the resistor body;

d) forming a field plate 36 (fig. 6 and col. lines 51-53) comprising polysilicon (**as recited in claim 37**) on the first insulating layer and approximately coextensive therewith and with the resistor body, the field plate having a top surface and a bottom surface, with a portion of the bottom surface 39-2 extending through the contact window in the first insulating layer and into contact with the first contact region of the resistor;

e) depositing a second insulating layer 42, with a first portion of the second insulating covering the field plate,

f) depositing a metal layer 44, with a portion of the metal layer covering the first portion of the second insulating layer,

g) patterning said portion of the metal layer to form

i) an electrical contact 44-1/44-2/44-3 to the top surface of the field plate, and a plurality of metal conductors 44-4/44-5 (figs. 9 and 10) formed on the first portion of the second insulating layer.

Re claim 38, Kondo discloses first (oxide film under layer 33, not shown; see lines 46-49) and second 42 insulating layers comprising SiO_2.

Re claim 39, Kondo discloses forming an insulative spacer 38 formed around the field plate.

Re claim 41, Kondo discloses an electrical contact 44-2 to the top surface of the field plate overlying the portion of the bottom surface of the filed plate that extends through the

portion of the bottom surface of the field plate that extends through the contact window in the first insulating layer and into contact with the first contact region 40-1 of the resistor.

Re claim 42, Kondo discloses the metal layer being additionally patterned to form an electrical contact 44-3 to the second contact region 40-2 of the resistor.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ahmed Sefer whose telephone number is (571)272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. Sefer/
Primary Examiner
Art Unit 2826